

SANYO Semiconductors

DATA SHEET

Thick Film Hybrid IC

STK4044V-

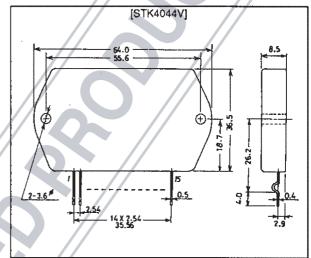
AF Power Amplifier (Split Power Supply) (100W min, THD = 0.08%)

Features

- · Compact packaging supports slimmer set designs
- Series designed from 20 up to 100 W (200 W) and pincompatibility (120 to 200 W have 18 pins)
- Simpler heat sink design facilitates thermal design of slim stereo sets
- Current mirror circuit application reduces distortion to 0.08%
- Supports addition of electronic circuits for thermal shutdown and load-short protection circuit as well as pop noise muting which occurs when the power supply switch is turned on and off

Package Dimensions

unit: mm 4075



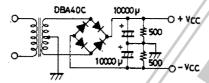
Specifications

Maximum Ratings at Ta = 25°C			Unit
Maximum supply voltage	V _{CC} max	±73	V
Thermal resistance	0 ј-с	1.1	°C/W
Junction temperature	Tj //	150	°C
Operating substrate temperature	Tc //	125	°C
Storage temperature	Tstg	-30 to +125	°C
Available time for load shorted	$V_{CC}=\pm 51 \text{ V}, R_L=8\Omega, f=50 \text{ Hz}, P_O=100 \text{ W}$	1	S
Recommended Operating Conditions at Ta = 25°C			Unit
Recommended supply voltage	v_{cc}	±51	V
Load resistance	R_L	8	Ω

Operating Characteristics at Ta = 25°C, V_{CC} = $\pm 51V$, R_L = 8Ω , VG = 40dB, Rg = 600Ω , 100k LPF ON, R_L (noninductive)

	_		min	typ	max	Unit
Quiescent current	I_{cco}	V _{CC} =±61V	15		120	mA
Output power	P_{O}	THD = 0.08% , $f = 20$ Hz to 20 kHz	100			W
Total harmonic distortion	THD	$P_0=1.0W$, $f=1kHz$			0.08	%
Frequency response	f_L , f_H	$P_0 = 1.0W, +0 dB$		20 to 50k		Hz
Input resistance	\mathbf{r}_i	$P_{O}=1.0W$, $f=1kHz$		55		kΩ
Output noise voltage	V _{NO} *2	$V_{CC}=\pm61V$, $Rg=10k\Omega$			1.2	mVrms
Neutral voltage	v_{N}	V _{CC} =±61V	-70	0	+70	mV

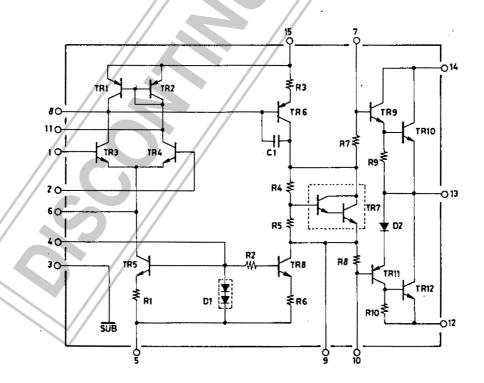
- Use rated power supply for test unless otherwise specified.
- *1 When measuring available time for load shorted and output noise voltage, use transformer power supply indicated below.
- *2 Output noise voltage represents the peak value on the rms scale (VTVM). The noise voltage waveform does not include the pulse noise.



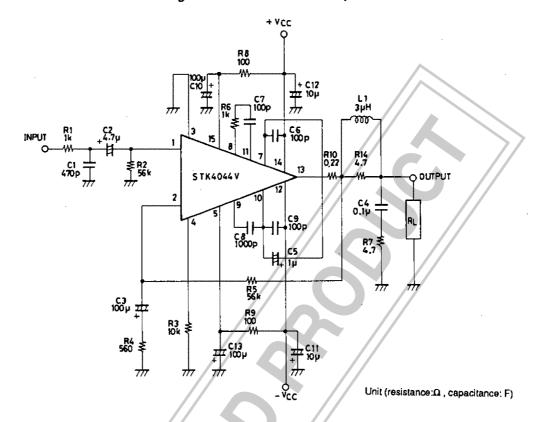
Specified Transformer Power Supply (MG-200 Equivalent)

Unit (resistance: Ω , capacitance: F)

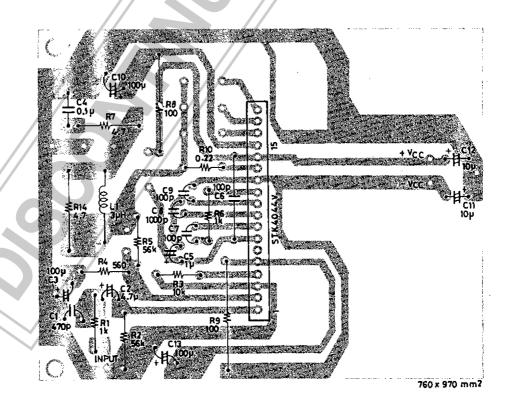
Equivalent Circuit



Sample Application Circuit: 100W min Single-Channel AF Power Amplifier



Sample Printed Circuit Pattern for Application Circuit (Copper-folled side)



Unit (resistance: Ω , capacitance: F)

Description of External Parts

 R_1, C_1 : Input filter circuit

· Reduces high-frequency noise.

C₂: Input coupling capacitor

 DC current suppression. A reduction in reactance is effective because of increases in capacitor reactance at low frequencies and 1/f noise dependence on signal source resistance which result in output noise worsening.

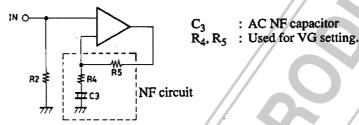
R₂: Input bias resistor

· Biases the input pin to zero.

• Affects V_N stability (refer to NF circuit).

• Due to differential input, input resistance is more or less determined by this resistance value.

 R_4, R_5 : NFB circuit (AC NF circuit). Use of resistor with 1% error is suggested. $C_3(R_2)$



VG settings are obtained using R₄ and R₅ according to the following equation:

$$log 20 \cdot \frac{R_5}{R_4}$$
 40 dB is recommended.

 Low-frequency cutoff frequency settings are obtained using R₄ and C₃ according to the following equation:

$$f_L = \frac{1}{2\pi \cdot R_4 \cdot C_3} \quad [Hz]$$

When changing the VG setting, you should change R_4 which requires a recheck of the low cutoff frequency setting. When the VG setting is changed using R_5 , the setting should ensure R_2 equals R_5 so that V_N balance stability is maintained. If the resistor value is increased more than the existing value, V_N balance may be disturbed and result in deterioration of V_N temperature characteristics.

R₃: Differential constant-current bias resistor

R₆, R₇ : For oscillation suppression and phase compensation applications (For use with differential stage applications)

: For oscillation suppression and phase compensation applications

(A Mylar capacitor is recommended for C₄ for use with output stage applications)

 C_6, C_9 : For oscillation suppression and phase compensation applications

Power stage (Must be connected near the pin) C₆: Positive (+) power C₉: Negative (-) power

C₈: For oscillation suppression and phase compensation applications (Oscillation suppression before power step clip)

C₅: For oscillation suppression and distortion improvement applications

R₈, C₁₀: Ripple filter circuit on positive (+) side.
 R₉, C₁₃: Ripple filter circuit on negative (-) side.
 C₁₁, C₁₂: For oscillation suppression applications

Used for reducing power supply impedance to stable IC operation and should be connected near the IC
pin. We recommend that you use an electrolytic capacitor.

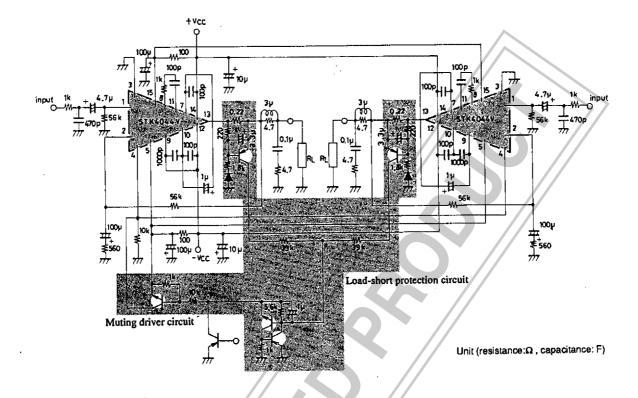
R₁₀ : Output resistor

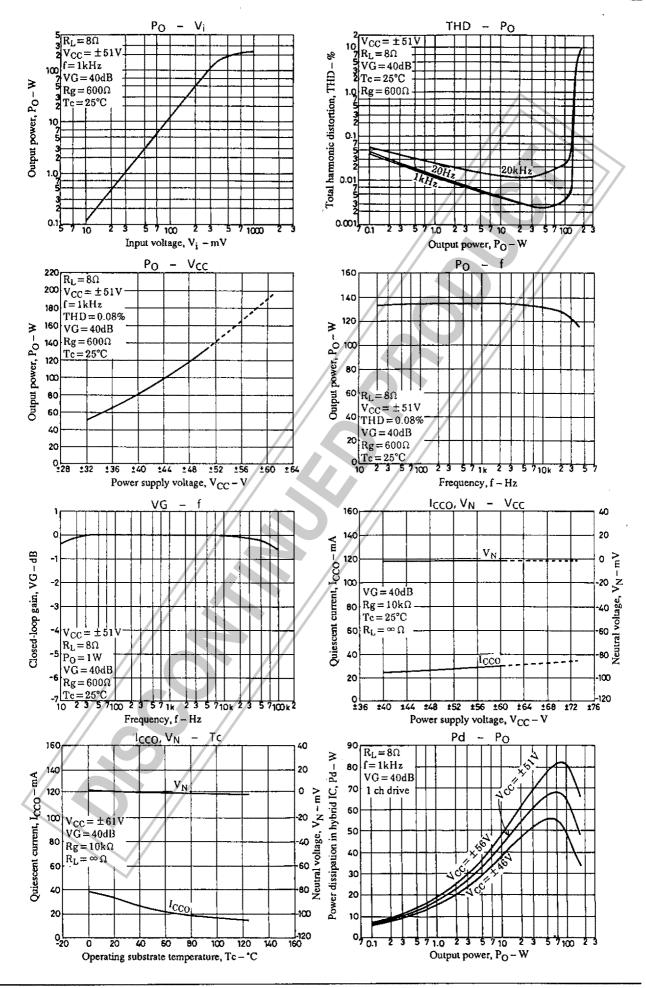
R7, C4

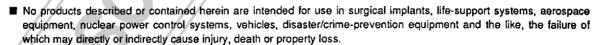
Increases load short handling capability during times of high output.

R₁₄, L₁: For oscillation suppression applications
Increases oscillation stability against capacitance loads.

Sample Application Circuit (Protection circuit and muting circuit)







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