NEC

MOS FIELD EFFECT TRANSISTOR
2SK3918

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3918 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

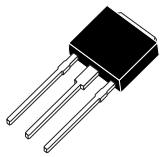
ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3918	TO-251 (MP-3)
2SK3918-ZK	TO-252 (MP-3ZK)

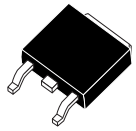
FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 7.5 mΩ MAX. (V_{GS} = 10 V, I_D = 24 A)
- Low C_{iss}: C_{iss} = 1300 pF TYP.
- 5 V drive available

(TO-251)



(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	25	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±48	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±192	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	29	W
Total Power Dissipation	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Single Avalanche Current Note2	I_{AS}	22	A
Single Avalanche Energy Note2	E_{AS}	48	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 12.5 V, R_G = 25 Ω, V_{GS} = 20 → 0 V

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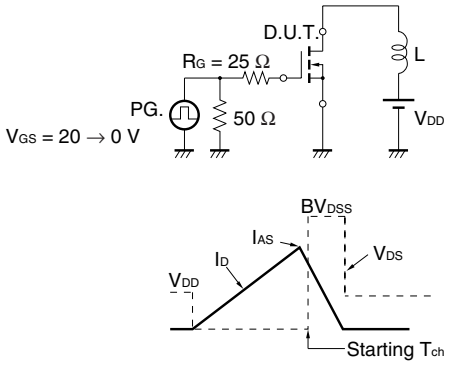
The mark ★ shows major revised points.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

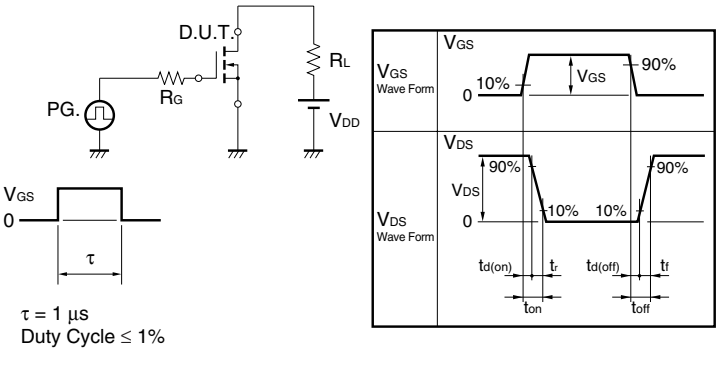
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	2.0	2.5	3.0	V
Forward Transfer Admittance **Note**	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 12 A	6	12		S
Drain to Source On-state Resistance **Note**	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 24 A		5.9	7.5	mΩ
	$R_{DS(on)2}$	V_{GS} = 5.0 V, I_D = 12 A		11	22.2	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		1300		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		310		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		220		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 12.5 V, I_D = 24 A		13		ns
Rise Time	t_r	V_{GS} = 10 V		14		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		38		ns
Fall Time	t_f			14		ns
Total Gate Charge	Q_G	V_{DD} = 20 V		28		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		5		nC
Gate to Drain Charge	Q_{GD}	I_D = 48 A		10		nC
Body Diode Forward Voltage **Note**	$V_{F(S-D)}$	I_F = 48 A, V_{GS} = 0 V		0.98		V
Reverse Recovery Time	t_{rr}	I_F = 48 A, V_{GS} = 0 V		27		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		15		nC

Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE